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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,976	NOE, AMANDA	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-27 are pending in the Application.

Claims 1, 8 and 24 have been amended.

Claims 1-27 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 6 August 2007 in response to the Office action mailed on 12 April 2007 have been fully considered. Though one of Applicant's arguments with respect to both claim 1 and claim 8 is persuasive, the remaining arguments are not persuasive for the reasons stated below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

More specifically, newly amended claim 1 recites, "inputting the parallel bits into a content addressable memory and a first register during a single clock cycle". Examiner is unable to find support for this new limitation in Applicant's original specification. In fact, paragraph 0061of the specification directly contradicts this newly added limitation (i.e. delaying the input to the first register by one clock cycle).

Claims 2-7 are rejected for inheriting the deficiencies of claim 1.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "the parallel output of the shift register" in lines 8-9 of the claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, "a parallel output of the shift register" is not previously set forth in the claim. Which output is being claimed here?

Claims 9-23 are rejected for inheriting the deficiencies of claim 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg (US PG Publication 2002/0159483 A1) in view of Craft (US Patent 5,652,878), and in further view of Agrawal et al. (US Patent 6,919,736 B1), hereinafter Agrawal.

As for claim 24, Clauberg teaches a method comprising:

deserializing an input serial data stream into a first parallel word (paragraph 0024, lines 1-3 - data is transformed into parallel bits. Note in paragraph 0024, all lines, though a 16-bit (i.e. 1 word) serial stream is used as an illustrative example, more bits (i.e. 2 words (32-bits)) maybe used. The first word (i.e. bits 0-15 in the 32-bit example) is deserialized);

storing the first parallel word in a register (Fig. 2, the deserializer feeds the parallel data into a register (element 214) via the demux (element 212) – paragraph 0032, lines 1-17).

deserializing the input serial data stream into a second parallel word (bits 16-31 (of the 32-bit example) are deserialized – paragraph 0032, lines 1-17).

grouping the first parallel word and the second parallel word into a plurality of data word subsets (Fig. 2, the output of the demux groups the first and second parallel words and send them to the register (element 214));

generating a third parallel word from the combination of the first and second parallel word, wherein the third parallel word is wider than the first parallel word and the second parallel word (the output (third parallel word –

element 204) consists of data larger than 32-bits, which was comprised in part by the combination of the first and second words); and

detecting a frame alignment symbol within the third parallel word by comparing a bit pattern of the third parallel word to a plurality of frame alignment patterns stored in a memory (the alignment position (i.e. symbol) is contained in the 192-bit portion of the data stream, which is subsequently sent to the extracting unit (paragraph 0027, all lines).

Though Clauberg teaches comparing a bit pattern of the third parallel word to a plurality of frame alignment patterns stored in a memory, he fails to teach the memory as being specifically a CAM. Though it is well known in that art that Clauberg could use any sort of common memory to store and compare his outgoing data (i.e. a RAM), he still fails to teach or suggest specifically using a CAM. Additionally, Clauberg teaches each of the fixed frame alignment patterns as being part of a respective one of a set of parallel words (Clauberg specifically teaches aligning parallel data in accordance to specific patterns/protocols).

Craft however teaches a method and apparatus of compressing data, which includes a circuit for storing incoming data (col. 2, lines 59-63). More specifically, Craft teaches implementing his circuit by use of a CAM rather than a RAM (col. 3, lines 42-50).

Craft further teaches selecting one of the parallel bit output formats to output based on match flag outputs from the CAM (i.e. comparison to fixed frame alignment patterns), wherein the match flag outputs are generated in response to the inputs to the

CAM (col. 5, lines 1-9 – a plurality of entries are stored in the CAM array, match flag signals (342) are generated based on the comparison of the data stored in the CAM with the data in the input buffer).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to store his outputted parallel data into the CAM as taught by Craft, rather than a standard means, such as with a random access memory. By doing so, Clauberg would benefit by improving the compressing ratio of the stored data, and increase throughput during transmission of the data as taught by Craft in col. 3, lines 50-57.

Additionally, though the combined teaching of Clauberg and Craft disclose grouping the second parallel word into a plurality of subsets, they fail to teach the data lines forming that bus as being grouped into a plurality of overlapping subsets of the bus, each containing at least one common data line as recited in the claim.

Agrawal however teaches an FPGA device having embedded memory with configurable depth and width in which he discloses overlapping the bits of the configurable memory block on a common shared interconnect bus (see the abstract and col. 12, lines 45-53 – the bits of the wide words of each memory block share interconnect buses on a overlapping basis)

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to further include Agrawal's FPGA device with configurable memory into his own frame byte alignment unit. By doing so, Clauberg's system would benefit by having a more versatile and efficient storage unit for storing data from his

output data stream. This memory would be capable of concatenating memory partitions, which would otherwise operate independently as taught by Agrawal in col. 3, lines 14-37. Additionally, Clauberg could benefit by exploiting the advantages of using Agrawal's memory as either a FIFO or LIFO device for data streams which is extremely beneficial to speed critical data as taught by Agrawal in col. 2, lines 49-64.

As for claim 25, Clauberg teaches selecting one of the subsets associated with a respective one of the frame alignment patterns that match the frame alignment symbol (paragraph 0028 – all lines. Sequence is output once alignment is identified).

As for claim 26, Clauberg teaches detecting the frame alignment symbol within one clock cycle (paragraph 0028, all lines. Clauberg teaches locating the alignment within one cycle).

As for claim 27, though Clauberg teaches grouping the second parallel word as comprising outputting the second parallel word, he fails to teach grouping them on a data bus that includes subsets of data lines that correspond to the data word subsets.

Agrawal however teaches an FPGA device having embedded memory with configurable depth and width in which he discloses overlapping the bits of the configurable memory block on a common shared interconnect bus corresponding to data word subsets (see the abstract and col. 12, lines 45-53 – the bits of the wide words of each memory block share interconnect buses on a overlapping basis)

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to further include Agrawal's FPGA device with configurable memory into his own frame byte alignment unit. By doing so, Clauberg's system would

benefit by having a more versatile and efficient storage unit for storing data from his output data stream. This memory would be capable of concatenating memory partitions, which would otherwise operate independently as taught by Agrawal in col. 3, lines 14-37. Additionally, Clauberg could benefit by exploiting the advantages of using Agrawal's memory as either a FIFO or LIFO device for data streams which is extremely beneficial to speed critical data as taught by Agrawal in col. 2, lines 49-64.

Response to Arguments

6. Applicant's amendments and arguments have been fully considered. Though one of Applicant's arguments with respect to both claim 1 and claim 8 is persuasive, the remaining arguments are not persuasive for the reasons stated below.

As for claim 1, Applicant's contends that the "[c]ombination [of Clauberg, Craft and Agrawal] inputs bits into CAM and [a] first register in different clock cycles". More specifically, Applicant asserts, "the parallel bits are first input into the register 214 and then at least several clock cycles later the data is input into storage unit 222. *Id.*, paragraph 27. Thus, Clauberg does not teach or suggest "*inputting the parallel bits into a content addressable memory and a first register during a single clock cycle,*" as recited by claim 1."

Examiner finds this argument persuasive, and therefore withdraws the § 103(a) set forth in the previous Office action.

Applicant additionally asserts with respect to claim 1, the "[c]ombination does not alter [the] alignment mechanism of Clauberg". More specifically, Applicant asserts, "a

combination of Craft with Clauberg would add the compression scheme of Craft to the aligned output data of Clauberg so that bandwidth may be more efficiently used. The newly stored data would not have any particular alignment associated with it and would not convey alignment information, but would simply be used to identify data that may be sent as a token as opposed to actual data. Even as noted by the Office Action at page 5, the output of Clauberg "is of a particular type and alignment," which suggests that the alignment would need to have already been detected. Accordingly, the combination does not teach or suggest "*wherein at least one of the set of parallel words includes a fixed frame alignment detection pattern having a data position*," as recited by claim 1."

This argument however is not persuasive, as Examiner addressed a similar argument in the "Response to Arguments" section of the Office action mailed 12 April 2007 (page 18, line 13 through page 19, line 5).

Applicant additionally asserts with respect to claim 1, the "[c]ombination does not does not have a bus that receives parallel bits and output of first register and that has overlapping subsets with at least one common data line". More specifically, Applicant asserts, "[f]irst, Agrawal teaches that the different interconnects may be used to transfer data in different directions, which is why there is shared (overlapping) use. *Id.*, col. 12 lines 23-27. However, Clauberg requires that data is sent only in one direction, i.e. from input to output. Thus, the concepts are not transferable and the inventions would not be combined."

This argument however is not persuasive. Examiner maintains as per the rejection set forth *supra*, that it would have been obvious for Clauberg to further include

Agrawal's FPGA device with configurable memory into his own frame byte alignment unit. Further, assuming *arguendo* that Clauberg only teaches uni-directional data transfer as alleged by Applicant, one of ordinary skill in the would understand that uni-directional data transfer does not necessarily preclude bus overlapping, Applicant's arguments notwithstanding.

Applicant additionally asserts, "[s]econdly, each of the LOSMs 281-284 do not have lines that are part of another LOSM, and thus they do not overlap. *Id.*, FIG. 2B and col. 12 lines 12-35. It is the use of the LOSMs that overlaps and not the LOSMs themselves. This is evident in that the subsets service completely separate I/O terminals. *Id.* In contrast, claim 1 recites "wherein the data lines forming the bus are grouped into a plurality of overlapping subsets.""

This argument however is not persuasive, as Examiner maintains that Agrawal *explicitly* teaches overlapping bits of the configurable memory block on a common shared interconnect bus corresponding to data word subsets (see previously cited abstract, and col. 12, lines 45-53).

Applicant additionally asserts, "[a]lso, as is plainly apparent from FIG. 2B, LOSMs 281-284 do not all share a common data line. *Id.*, FIG. 2B and col. 12 lines 12-35. In contrast, claim 1 recites "*wherein the data lines forming the bus are grouped into a plurality of overlapping subsets*" of the bus that each contain at least one common data line.""

This argument however is not persuasive, as Examiner addressed a similar argument in the "Response to Arguments" section of the Office action mailed 12 April 2007 (page 19, lines 10-18).

Lastly, Applicant contends, "[a]dditionally, Agrawal would not change the structure of the registers of Clauberg, which does not have "*a bus configured to receive the parallel bits and output of the first register*," as recited in claim 1. In Clauberg, one bus receives the parallel bits and transmits them to the register 214 and a different second bus transfers the output of register 214 to register 216."

This argument however is not persuasive, as Examiner maintains that the bus, as presently recited, does not require actually receiving the parallel bits and output of the first register (notice the "configured to" language used in this method claim). Additionally note, the output of the first register contains bits that are, in part, reordered parallel bits from the deserializer. In other words the output of the first register of Clauberg contains the parallel bits.

Applicant's argument that claims 2-7 are allowable for further limiting claim 1 is not persuasive. More specifically, though no art rejections presently exist against claim 1, it still remains rejected under § 112(1).

As for claim 8, Applicant's argument that "any combination would [not] have the CAM receiving the first parallel data output and the output of the shift register in parallel" is persuasive.

Applicant's remaining argument with respect to claim 8 is not persuasive as per the arguments of claim 1, *supra*.

Applicant's argument that claims 9-23 are allowable for further limiting claim 8 is not persuasive. More specifically, though no art rejections presently exist against claim 8, it still remaining rejected under § 112(2).

Applicant's remaining arguments with respect to claim 24 are not persuasive as per the arguments of claim 1, *supra*.

Applicant's argument that claims 25-27 are allowable for further limiting claim 24 is not persuasive. More specifically, claim 24 still remains rejected under § 103(a) as per the rejections *supra*.

Applicant's arguments with respect to claims 2, 9, 13 and 21 are rendered moot, as no art rejections are presently asserted against their respective base claims.

Allowable Subject Matter

7. Claims 8-23 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. More specifically, neither Clauberg (US PG Publication 2002/0159483 A1), nor Craft (US Patent 5,652,878), nor Agrawal et al. (US Patent 6,919,736 B1), teach (either alone or in combination), "a content addressable memory that is coupled to an output of the shift register and that receives the first parallel data output *in parallel* with the parallel output of the shift register" (emphasis added).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

9/13/07